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Chernihiv Polytechnic National University



Erasmus+ Project 101127683 — DIGITRANS

Digital transformation of HEIs education process in Ukraine and Moldova for sustainable engagement with enterprises

Volodymyr Kazymyr, Dr. in Comp. Sc., prof.,

<https://stu.cn.ua/en/>

Kick-off meeting,
January 11, 2024, RTU



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Base structure for the project: Institute of Electronic and Information Technologies

Department	Specialty
Electrical Engineering and Information Measuring Technologies	Electrical engineering and electromechanics
Electronics, Automation, Robotics and Mechatronics	Electronics
Radio Engineering and Embedded Systems	Electronic communications and radio engineering
Information and Computer Systems	Computer Engineering
Information Technologies and Software Engineering	Software Engineering
Cyber Security and Mathematical Modeling	Cyber Security

Education levels: bachelor (4 years – 800 students), master (1.5 years – 200 students),
PhD (4 years – 50 post graduate students)

Partner companies:





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CPNU project team

- **Project manager/coordinator**
 - **Volodymyr Kazymyr, DSc., professor, professor of Information and Computer Systems department**
- **Teachers:**
 - **Sergey Ivanets, PhD, as. prof., director of electronic and information technology institute**
 - **Oleksandr Veligorsky, head of Radio Engineering and Embedded Systems department**
 - **Maksym Khomenko, PhD, as. prof., Radio Engineering and Embedded Systems department Department**
 - **Andrii Rogovenko, PhD, as. prof., Information and Computer Systems department**
 - **Oleksandr Drozd, senior lecture, Information and Computer Systems department**
- **Technical support**
 - **Dmytro Susa, director of Educational-Scientific Information Computing Center**
 - **Baida Vladyslav, PhD student**
- **Finance manager**
 - **Natalia Gaidai, accountant**

WP3: Development of Sharing Remote Experiment Environment (SREE)

Particular objectives

- to develop the Sharing Remote Experiment Environment (SREE) platform for on-line laboratory works with physical equipment of remote laboratories for learning and teaching practical topics in computer and electronic engineering
- to integrate SREE with Sharing Modelling and Simulation Environment (SMSE) that affords virtual laboratories based on open software kernels using Jupyter Notebooks, for resulting acquisition and piloting of Digital Learning Ecosystem (DLE)
- to create methodology of implementing and sharing remote applications of the HEIs laboratories' equipment and software tools for distance usage in framework of DLE based on application of ICT tools

Outcomes

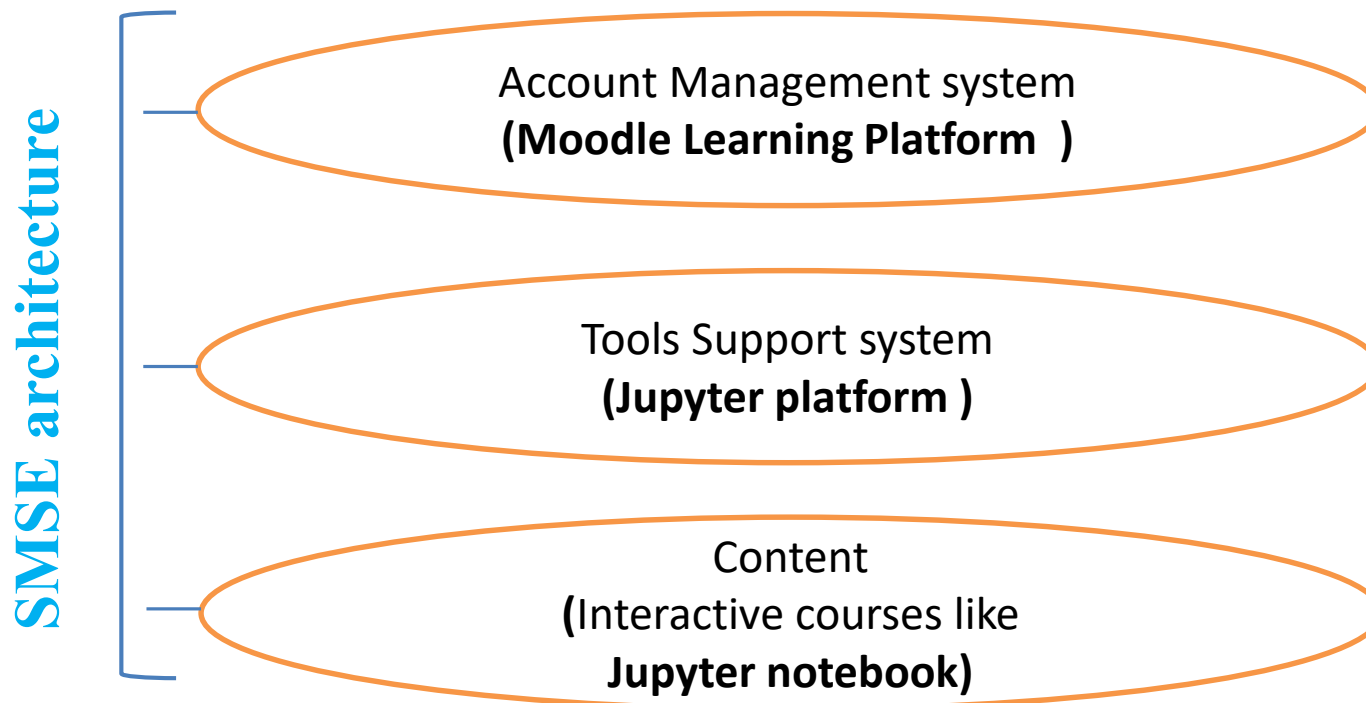
	<i>Deliverables</i>	<i>Month</i>
D3.1	Development of a concept of the SREE	3
D3.2	Development of the SREE technical platform and SREE web interface	12
D3.3	Creation of two laboratories with physical Equipment	20
D3.4	Integration of SREE with LMS Moodle and SMSE in DLE	24
D3.5	Development of methodical documents to acquisition and piloting of SREE in framework of DLE	27

Shared Modelling and Simulation Environment (SMSE)

Developed during Erasmus+ project: **CybPhys - Development of practically-oriented student-centred education in the field of modelling of Cyber-Physical Systems (2019-2023)**

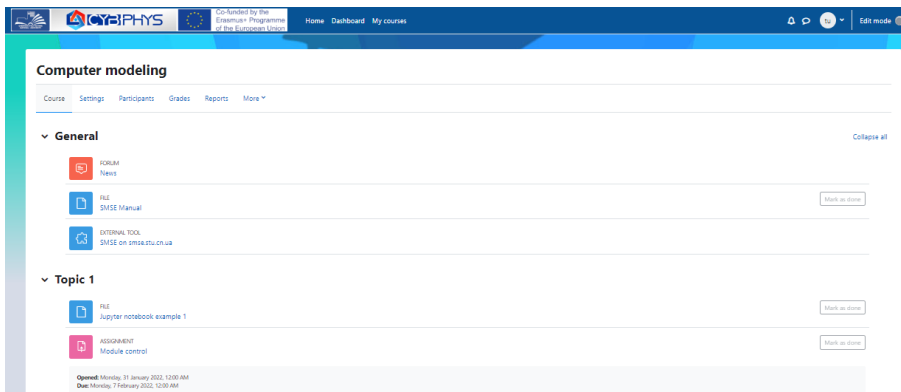
The aim of SMSE - to provide on-line training of student with practical skills in modelling and simulation of Cyber-Physical Systems using different program kernels

SMSE Idea – embedding Jupyter platform to Moodle

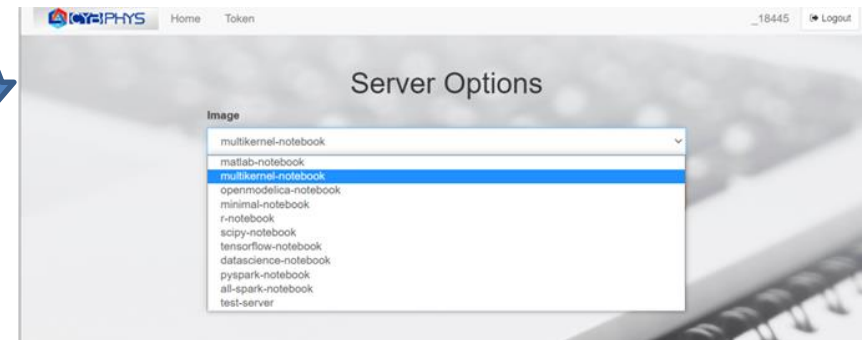


SMSE provides use of SOFTWARE TOOLS in on-line mode

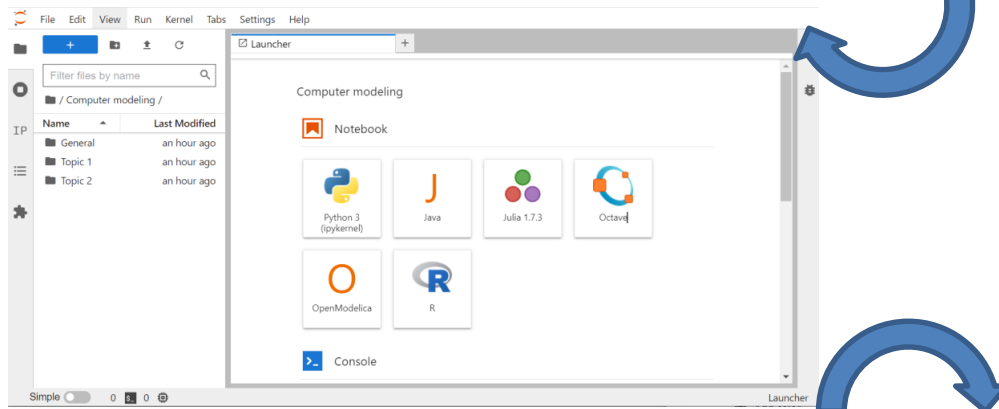
Moodle course



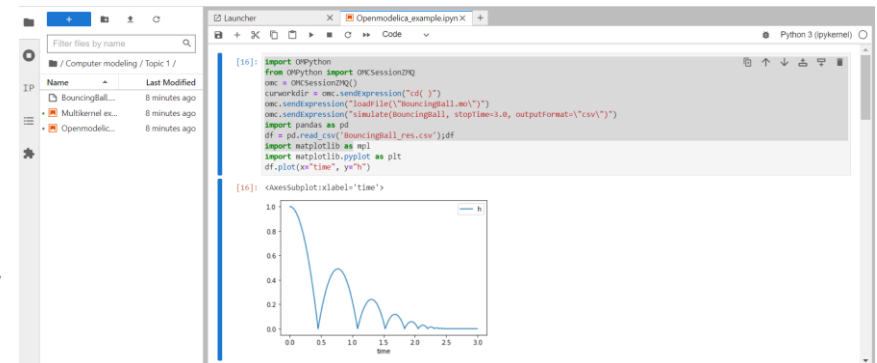
Select virtual server on Jupyter Hub



Start Jupyter Lab



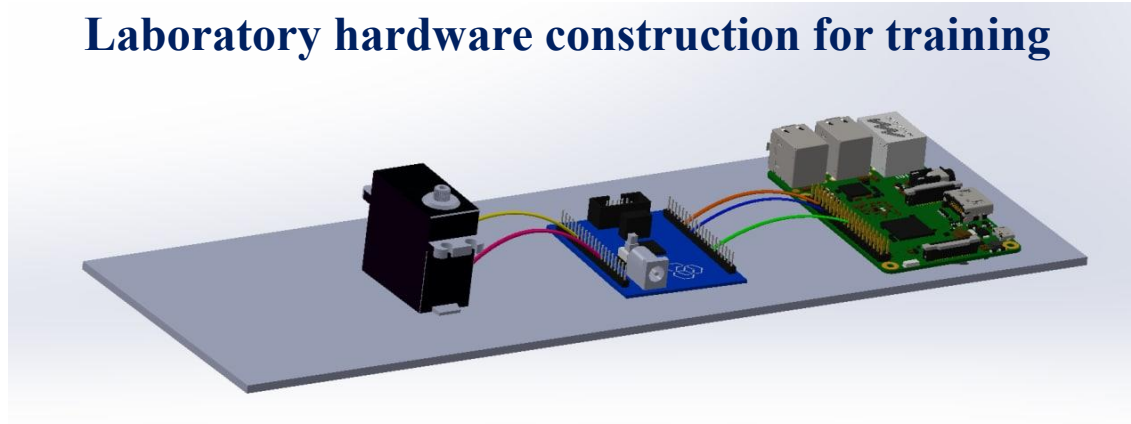
Open and run Jupyter Notebook



Our aim - to expand it to HARDWARE DEVICES

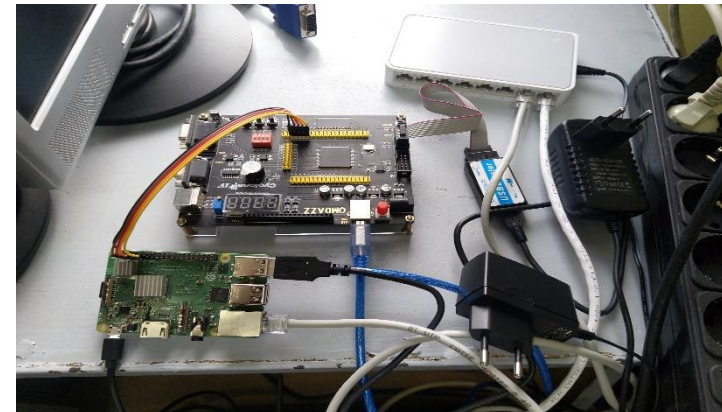
Sharing Remote Experiment Environment (SREE)

Laboratory hardware construction for training

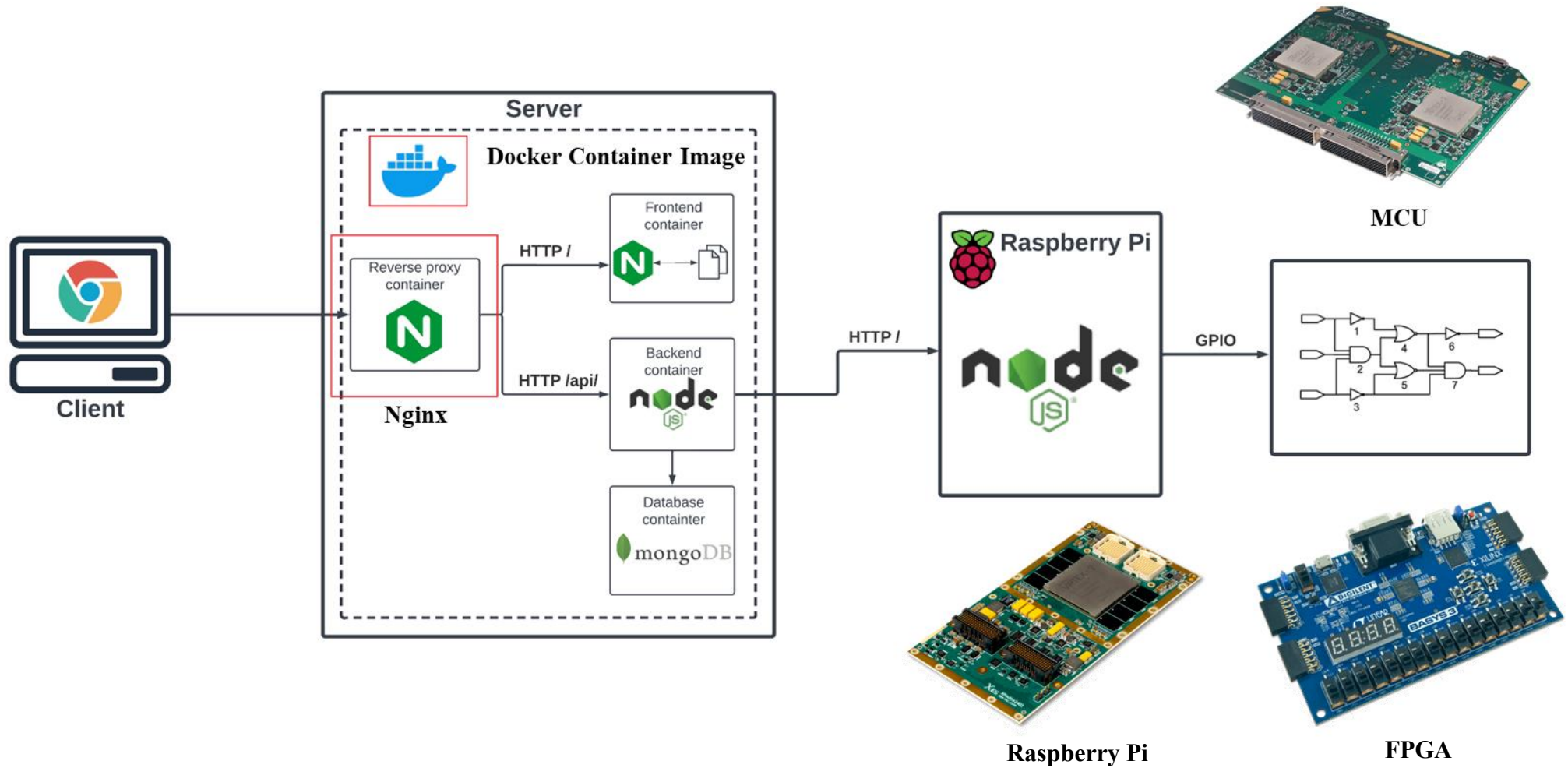


Right to Left: Raspberry Pi, FPGA demo board , servo motor as a peripheral device

The aim of SREE is to access it via SMSE remotely in on-line mode

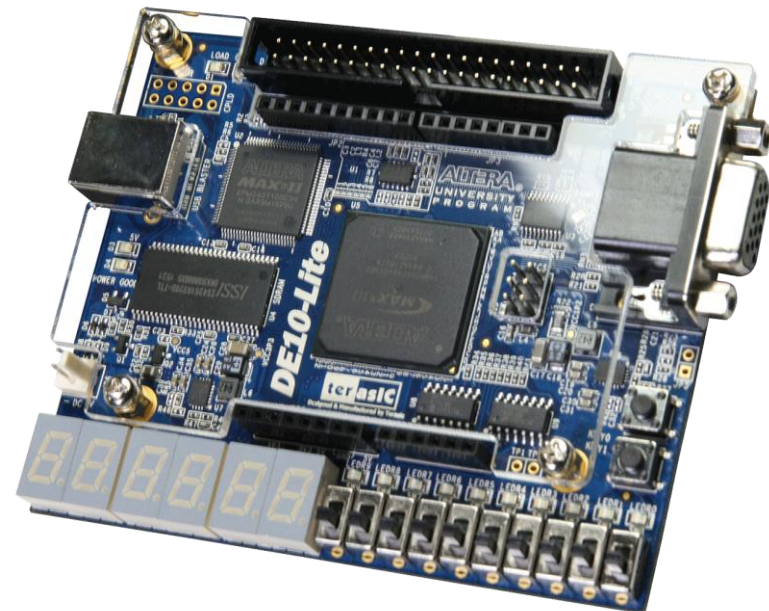


SREE platform concept



User task - FPGA programming

```
module up_counter(input clk, reset,  
output[3:0] counter  
);  
reg [3:0] counter_up;  
  
always @(posedge clk or posedge reset)  
begin  
if(reset)  
counter_up <= 4'd0;  
else  
counter_up <= counter_up + 4'd1;  
end  
assign counter = counter_up;  
endmodule
```



Control Panel View

File Settings

Hello, Nikita Poberezsky

Choose board:
Terasic DE0-Nano

Start Debug Stop Debug

Start debug after FPGA flashing

Choose Sequence Of Signals File

Send Sequence Of Signals File


Start Sequence Of Signals

Start sequence with debug

Debug time discreteness:
1 s

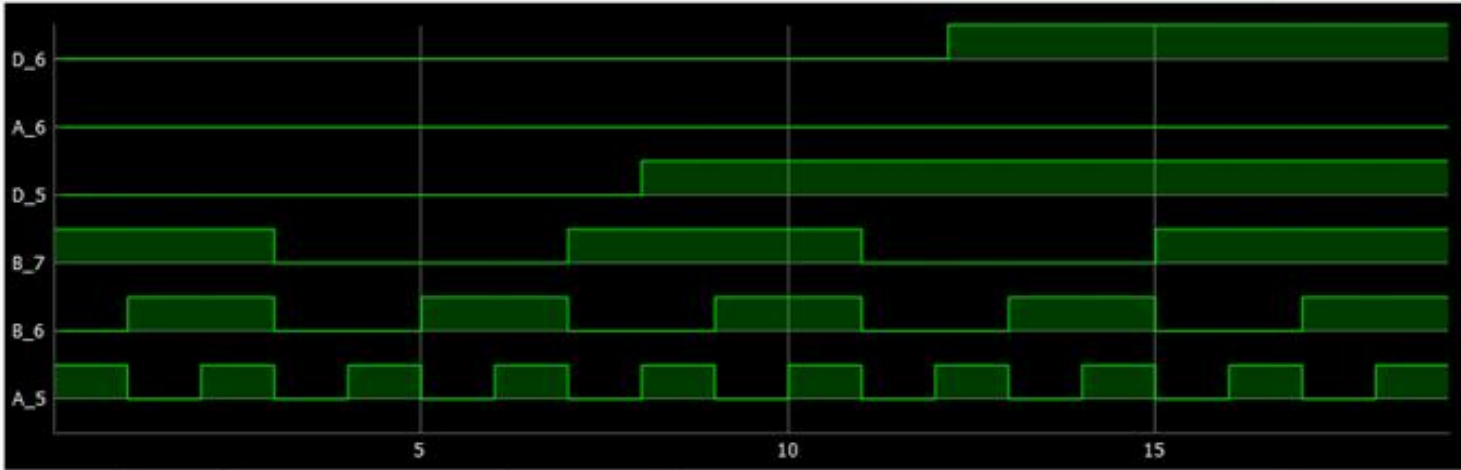
Debug time limit, s

FPGA Inputs:
D_5 A_6 D_6



As window Attach cursor to axis

500 ms Change Settings

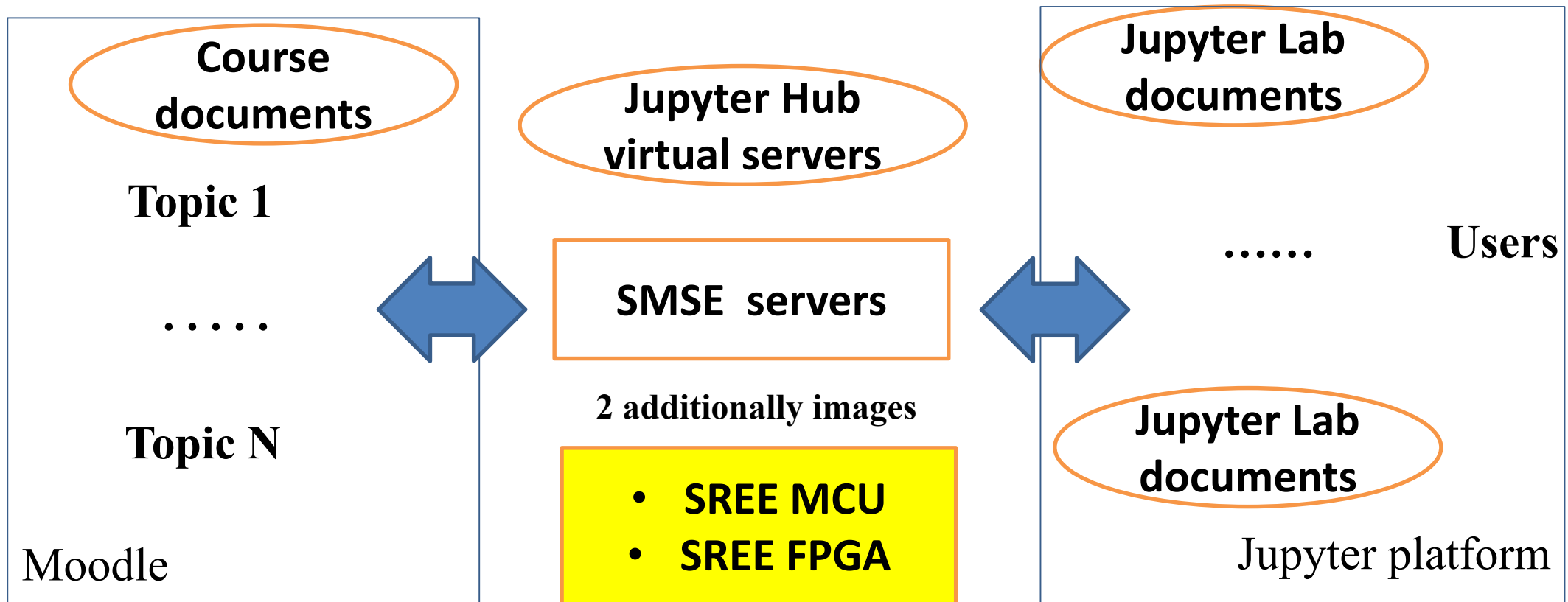


Full scale Clear Select Displayable Pins Measurement Save waveform

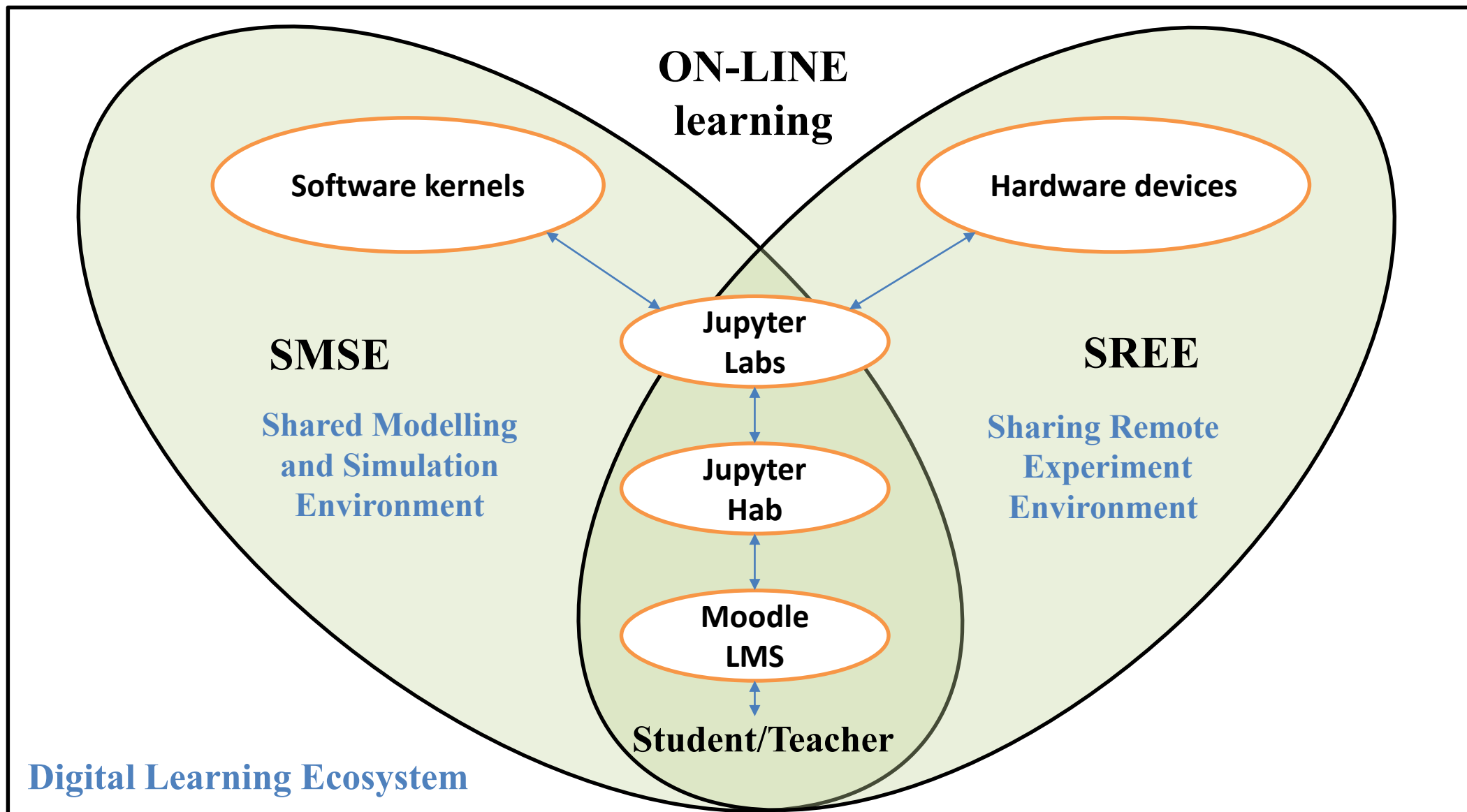
Send Firmware Choose Firmware

Logout

Integration of SREE with SMSE in DLE

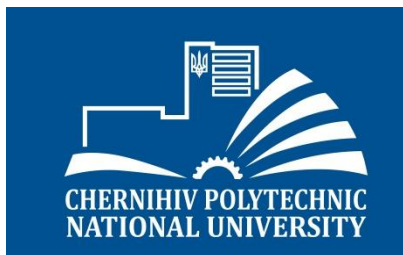


Digital Learning Ecosystem (DLE)



Procurement plan for two laboratories of SREE

- **Server, routing equipment – 1 set;**
- **Single-board computers (Raspberry Pi 4) – 10 pcs;**
- **Development boards for digital design (FPGA boards) – 5 pcs;**
- **Development boards for microcontroller systems (MCU boards) – 5 pcs;**
- **Extension boards for Single-board computers – 10 pcs;**
- **Multi-function laboratory device (oscilloscope and ets) – 10 pcs;**
- **Electrical and electromechanic components – 10 sets;**
- **Printed circuit boards – 10 pcs;**
- **Webcam – 10 pcs;**
- **PCs – 10 set;**
- **Laptop – 1 pcs;**
- **APC Smart – 1 pcs.**



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